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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,878	06/25/2003	Hideo Oishi	60188-538	2253

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EXAMINER	
STEVENSON, ANDRE C	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,878	OISHI, HIDEO	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *1-3,7-9 and 13-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5,6,10,11,12,16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/17/03, 06/25/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

During a telephone conversation with M. Fogarty on April 20, 2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 4, 5, 6, 10, 12 and 16. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-3, 7-9 and 13-15 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 06/25/03 and 09/17/03 were filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims #4, 5, 6, 10, 11 and 12 are rejected under 35 U.S.C. 102(b) as being unpatentable by Smayling et al. (U.S. Pat. No.5,798,649, Patented 08/25/98, Filed 08/19/932).

Smayling substantially shows the claimed invention, as shown in figures 1-6 and corresponding text. **Pertaining to claim #4,** Smayling shows, method for carrying out a burn-in test on a great number of semiconductor devices that have been formed on a semiconductor wafer, each said device including a gate oxide film between a substrate and a gate electrode, the gate electrode being connected to a metal interconnect, wherein the method comprises the step of exposing the wafer to an electromagnetic wave as an alternating current wave and placing an electric field with a predetermined intensity on the gate oxide film of each said device on the wafer, thereby carrying out the burn-in test on the devices **(column #3, lines 60-67; column #4, lines 1-4; column #6, lines 24-55; column #2, lines 22-35)**. The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper. ***Pertaining to claim #5,*** Smayling shows, a method comprising the steps of: sensing a voltage stress imposed on the gate oxide film each said device while the wafer is being exposed to the electromagnetic wave; and controlling the intensity of the electric field, which is represented by the electromagnetic wave generated, so that

the voltage stress sensed as being imposed on the gate oxide film falls within a preset threshold value range **(column #6, lines 24-55).** The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper. **Pertaining to claim #6,** Smayling shows, a method wherein the voltage stress, which has been sensed as being imposed on the gate oxide film, comprises a forward voltage- stress and a reverse voltage stress, and wherein the electric field intensity of the electromagnetic wave generated is controlled so that the forward and reverse voltage stresses imposed on the gate oxide film fall within first and second preset threshold value ranges, respectively, the second range being lower than the first range **(fig. #4-6; column #6, lines 40-67; column #7, lines 1-13**). The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper. **Pertaining to claim #10,** Smayling shows, a method for carrying out a

burn-in test on a great number of semiconductor devices that have been formed on a semiconductor wafer, each said device including a gate oxide film between a substrate and a gate electrode, the gate electrode being connected to a metal interconnect, wherein the method comprises the step of exposing the wafer to an electric field as an alternating current wave and setting the electric field placed on the gate oxide film of each said device on the wafer to a predetermined intensity, thereby carrying out the burn-in test on the devices **(column #3, lines 60-67; column #4, lines 1-4; column #6, lines 24-55; column #2, lines 22-35).** ***Pertaining to claim #11,*** Smayling shows, a method comprising the steps of: sensing a voltage stress imposed on the gate oxide film of each said device while the wafer is being exposed to the electric field; and controlling the intensity of the-electric field generated so that the voltage stress sensed as being imposed on the gate oxide film falls within a preset threshold value range **(column #6, lines 24-55).** The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper. **Pertaining to claim #12,** Smayling shows, a method wherein the voltage stress, which has been sensed as being imposed on the gate oxide film, comprises, a forward voltage stress and a reverse voltage stress, and wherein the intensity of the electric field generated is controlled so that the forward and reverse voltage stresses imposed on the gate oxide film fall within first and second **(fig. #4-6; column #6, lines 40-67; column #7, lines**

1-13). The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim #16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling et al. (U.S. Pat. No.5,798,649, Patented 08/25/98, Filed 08/19/93) as applied to claim #4, 5, 6, 10, 11 and 12 above, and in view of Smith Jr. et al. (U.S. Pat. No.6,192,826, Patented 02/27/01, Filed 04/23/19).

Smayling substantially shows the claimed invention, as shown the corresponding text above. Smayling also shows, pertaining to **claim #16**, a method for carrying out a burn-in test on a great number of semiconductor devices that have been formed on a semiconductor wafer, each

said device including a gate oxide film between a substrate and a gate electrode, the gate electrode being connected to a metal interconnect, the method comprising the steps of: exposing the wafer to an electric field that has been generated as a direct current wave from a conductive plate; where the electric field generated from the conductive plate exists, to expose the wafer to the electric field intermittently, whereby the wafer is exposed to an alternating-current electric field to carry out the burn-in test on the device **(column #3, lines 60-67; column #4, lines 1-4; column #6, lines 24-55; column #2, lines 22-35)**. The Examiner notes that Smalying does not state explicitly an electromagnetic wave generating means nor an electric field. However, Smayling shows embodiments that uses both direct and alternating current. The Examiner takes the position that these currents produce moving charges (direct current; forward testing) (alternating current; forward and reverse testing) that produces an electromagnetic field and an electric field by their physical nature. These fields, as shown by Smayling in the above recited text, can be controlled by controlling the current applied to the test. For these reasons, the Examiner takes the position that the rejection is proper.

Smayling fails to show, with respect to claim #16, a method for loading and unloading a wafer into/from a space.

Smith teaches, in similar method for testing semiconductors, **pertaining to claim #16,** a method for loading and unloading a wafer into/from a space **(column #62, lines 24-51)**.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, with respect to **claim #16**, to include a method for loading and unloading a wafer into/from a space, in the method of Smayling, as taught by Smith, with the motivation

that a qualification wafer from a processed cassette may then be tested (destructively or non-destructively), while semiconductor devices may be formed from the production wafers

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure; Gutt et al. (U.S. Pat. No. 5,057,441), Kim (U.S. Pat. No. 5,548,884), Pedrotti et al. (U.S. Pat. No. 6,862,403), Malinoski et al. (U.S. Pat. No. 6,389,225), Dobashi et al. (U.S. Pat. No. 6,593,167), Lee et al. (U.S. Pat. No.5,940,680), Smayling et al. (U.S. Pat. No. 5,648,275).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

05/01/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER